IN THE CLAIMS:

1. An apparatus for monitoring an execution behavior of a program, comprising:

a processor for executing a plurality of instructions;

a probe logic unit in communication with the processor that generates probe signals representative of memory access misses occurring in the processor;

a performance monitor circuit element that receives the probe signals and associates a temporal identifier signal with the probe signals; and

a memory for storing the temporal identifier signal and the probe signals.

2. The apparatus of claim 1, comprising:

one or more memory devices;

wherein the probe generator generates probe signals in response to a memory access miss signal when executing a specified instruction.

3. The apparatus of claim 1, comprising:

a translation lookaside buffer (TLB);

wherein the probe generator generates probe signals recording a TLB miss when executing a specified instruction.

4. The apparatus of claim 1, comprising:

the processor including a translation lookaside buffer (TLB) and a program counter, the TLB generating a TLB miss signal;

wherein the probe generator generates a program counter signal, a TLB identification signal indicating a miss in the TLB, a TLB miss count signal representing an accumulative count of TLB misses, and a time stamp signal when the TLB miss signal is activated.

5. The apparatus of claim 4, comprising:

the probe generator including a TLB miss counter coupled to the TLB miss signal, the TLB miss counter is incremented when the TLB miss signal is activated.

6. The apparatus of claim 1, comprising:

the processor including a first high-speed memory and a program counter, the first high-speed memory generating a first high-speed memory miss signal;

wherein the probe generator generates a program counter signal, a first high-speed memory miss signal indicating a miss in the first high-speed memory, a first high-speed memory miss count signal representing a number of misses in the first high-speed memory, and a time stamp signal when the first high-speed memory miss signal is activated.

7. The apparatus of claim 6, comprising:

the probe generator including a first high-speed memory miss counter coupled to the first high-speed memory miss signal, the first high-speed memory miss counter is incremented when the first high-speed memory miss signal is activated.

8. The apparatus of claim 1, comprising:

a second high-speed memory and a program counter, the second high-speed memory generating a second high-speed memory miss signal;

wherein the probe generator generates a program counter signal, a second high-speed memory miss signal indicating a miss in the second high-speed memory, a second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and a time stamp signal when the second high-speed memory miss signal is active.

9. A method for monitoring an execution of a program, the method comprising the steps of:

(1) obtaining a first instruction including a first address;

(2) searching a first memory device for an entry associated with the first address;

(3) when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device;

(4) generating a temporal identifier signal that is associated with the probe signals; and

(5) storing the temporal identifier signal and the probe signals in memory.

10. The method of claim 9,

step (1) including the step of incrementing a program counter with the first instruction; and

step (3) including the step of generating a second probe signal indicating a content of the program counter.

11. The method of claim 9,

before step (5),

searching a second memory device for an entry associated with the first address,

when the entry in the second memory device does not exist, generating at least one probe signal indicating a miss entry in the second memory device, and

generating a temporal identifier signal that is associated with the probe signal.

12. The method of claim 9,

before step (2),

searching an address storage device for an entry associated with the first address,

when the entry in the address storage device does not exist, generating at least one probe signal indicating a miss entry in the address storage memory device, and

generating a temporal identifier signal that is associated with the probe signal.